What is claimed is:

1. A trace data control circuit comprising:

a branch event generation circuit for outputting trace data related to a branch instruction in response to a branch instruction,

a CPU-access event generation circuit for outputting a trace data related to a data access instruction in response to a data access instruction,

a selection means capable of inputting at least trace data output from the branch-event generation circuit and trace data output from the CPU-access event generation circuit, and selecting trace data related to either one of these events,

a memory means for storing the trace data, and

a trace data abbreviation means that abbreviates one part of the trace data and outputs the partly abbreviated trace data,

wherein said branch event generation circuit further comprises an address abbreviation information generation means for detecting an overlapped portion of a branch-source address with a branch-destination address from the upper address bit sides thereof, and generating a branch-destination address abbreviation information.

2. The trace control circuit according to claim 1, wherein said branch-event generation circuit further comprises:

one or more than one first latching means for latching address data per predetermined number of bits respectively,

one or more than one second latching means for respectively delaying address data for predetermined base clock cycles from the first latching means and latching the delayed data per predetermined number of bits for each, and

one or more than one comparing means each for comparing the

data latched by the first latching means with the data latched by the second latching means per predetermined number of bits and outputting the result of the comparison to the address abbreviation information generation means.

3. The trace control circuit according to claim 2, wherein said trace data abbreviation means further comprises:

a register capable of reading out and storing a trace data related to one of trace events including said branch access event from the trace data abbreviation means,

a plurality of switching means disposed between a plurality of storing means composing said register and an output section of said trace data abbreviation means, and

a control means which is connected to a control terminal of each of the plurality of switching means and executes an on-off control per predetermined number of bits as a base unit for data abbreviation on the basis of the address abbreviation information.

4. A trace data control circuit comprising:

a branch event generation circuit for outputting trace data related to a branch instruction in response to a branch instruction,

a CPU-access event generation circuit for outputting a trace data related to a data access instruction in response to a data access instruction,

a selection means capable of inputting at least trace data output from the branch-event generation circuit and trace data output from the CPU-access event generation circuit, and selecting trace data related to either one of these events,

a memory means for storing the trace data, and

a trace data abbreviation means that abbreviates one part of the trace data and outputs the partly abbreviated trace data,

wherein the CPU-access event generation circuit further comprises an address abbreviation information generation means for detecting an overlapped portion of a preceding address to be accessed with a succeeding address to be accessed next from the upper address bit sides thereof, in the case of consecutive data access operation, and generating succeeding address abbreviation information.

5. The trace control circuit according to claim 4, wherein said CPU-access event generation circuit further comprises;

one or more than one first latching means for latching address data per predetermined number of bits for each,

one or more than one second latching means for delaying address data for a predetermined base clock cycles from the first latching means and latching per predetermined number of bits for each, and

one or more than one comparing means each for comparing the data latched by the first latching means with the data latched by the second latching means per predetermined number of bits and outputting the result of the comparison to the address abbreviation information generation means.

6. The trace control circuit according to claim 5, wherein said trace data abbreviation means further comprises:

a register capable of reading out and storing a trace data related to one of trace events including said CPU-access event from the trace data abbreviation means,

a plurality of switching means disposed between a plurality of storing means composing said register and an output section of

said trace data abbreviation means, and

a control means which is connected to a control terminal of each of the plurality of switching means and executes an on-off control per predetermined number of bits as a base unit for data abbreviation on the basis of the address abbreviation information.

7. A trace data control circuit comprising:

a branch event generation circuit for outputting trace data related to a branch instruction in response to a branch instruction,

a CPU-access event generation circuit for outputting a trace data related to a data access instruction in response to a data access instruction,

a selection means capable of inputting at least trace data output from the branch-event generation circuit and trace data output from the CPU-access event generation circuit, and selecting trace data related to either one of these events,

a memory means for storing the trace data, and

a trace data abbreviation means that abbreviates one part of the trace data and outputs the partly abbreviated trace data,

wherein said CPU-access event generation circuit further comprises one or more than one latching means for latching read or write data per predetermined number of bits respectively,

one or more than one comparing means each for comparing bit strings held by said one or more than one latching means per predetermined number of bits with a predetermined abbreviation target bit string, and

a data abbreviation information generation circuit that inputs the result of the comparison output from said one or more than one comparing means and generates abbr viation information per

predetermined number of bits of data related to the read or write data.

8. The trace control circuit according to claim 7, wherein said trace data abbreviation means further comprises:

a register capable of reading and storing a trace data related to either one of said branch event or said CPU-access event from said memory means,

a plurality of switching means disposed between a plurality of storing means composing the register and an output section of said trace data abbreviation means, and

a control means that is connected to a control terminal of each of the plurality of switching means and executes an on-off control per a predetermined number of bits as a base unit for data abbreviation, on the basis of the address abbreviation information.